CLAIMS

What is claimed:

1. A multi-phase method of programming an array of non-volatile memory ("NVM") cells, said method comprising:

Applying to a first set of NVM cells first phase programming pulses; and

upon one or more NVM cells of the first set of cells reaching or exceeding a first intermediate threshold voltage level, applying to a terminal of one or more cells in the first set of cells second phase programming pulses adapted to induce relatively greater threshold voltage changes in cells having less stored charge than in cells having relatively more stored charge.

2. The method according to claim 1, wherein applying first phase programming pulses to one or more NVM cells of the first set of cells comprises applying to a terminal of one or more NVM cells of the first set of NVM cells incrementally increasing programming pulses in concert with pulses of substantially fixed voltage applied to gates of the one or more NVM cells; and

wherein applying second phase programming pulses, comprises applying to a terminal of the one or more cells programming pulses of substantially fixed voltage in concert with gate pulses of incrementally increasing voltage.

3. The method according to the claim 2, wherein applying to a terminals of the one or more cells of the first set second phase programming pulses of substantially fixed voltage in concert with gate pulses of incrementally increasing voltage is repeated until one or more of the cells of the first set reaches a first target threshold voltage level.

4. The method according to claim 3, wherein the second phase programming pulses of substantially fixed voltage are at a voltage

corresponding to the voltage of the programming pulse which first succeeded in raising the threshold voltage of one or more cells of said first set to or beyond the first intermediate threshold voltage.

5. The method according to claim 3, wherein the initial value of the second phase gate pulses are at a voltage corresponding to the gate voltage of the programming pulse which first succeeded in raising the threshold voltage of one or more cells of said first set to or beyond the first intermediate threshold voltage.

6. The method according to claim 4, wherein the NVM cell is a multi-level cell.

7. The method according to claim 6, further comprising applying to a terminal of one or more NVM cells of a second set of NVM cells to be programmed to a second target threshold voltage first phase programming pulses of incrementally increasing voltage in concert with pulses of substantially fixed voltage applied to a gate of each of said NVM cells of said second set, wherein the first programming pulse applied to a terminal of the one or more NVM cells in the second set has a voltage corresponding to the voltage of the programming pulse which first succeeded in raising the threshold voltage of a cell in the first set to or beyond the first intermediate threshold voltage.

8. The method according to claim 7, further comprising upon one or more NVM cells of said second set reaching or exceeding a second intermediate threshold voltage, applying to a terminal of one or more cells of the second set second phase programming pulses of substantially fixed voltage in concert with gate pulses of incrementally increasing voltage.

9. The method according to claim 8, wherein applying to a terminal of one or more cells of said second set second phase programming pulses of substantially fixed voltage in concert with gate pulses of incrementally increasing voltage is repeated until said cell of said second set reaches the second target threshold voltage.

10. The method according to claim 1, wherein first phase programming comprises applying to a terminal of one or more NVM cells of a first set of NVM cells incrementally increasing programming pulses in concert with pulses of substantially fixed voltage applied to a gate of the one or more NVM cells; and

wherein applying second phase programming pulses to one or more cells in the first set comprises applying to a terminal of the one or more cells programming pulses of incrementally increasing voltage in concert with gates pulses of a relatively reduced and substantially fixed voltage.

11. The method according to the claim 10, wherein applying to a terminal of one or more cells of a first set programming pulses of incrementally increasing voltage is repeated until all of the one or more cells of said first set reaches a first target threshold voltage.

12. The method according to claim 11, wherein the NVM cell is a multi-level cell.

13. The method according to claim 12, further comprising applying to a terminal of one or more NVM cells of a second set of NVM cells to be programmed to a second target threshold voltage first phase programming pulses of incrementally increasing voltage in concert with pulses of substantially fixed voltage applied to a gate one or more cells of the second set, wherein the first phase programming pulse applied

to a terminal of the one or more NVM cells in the second set has a voltage corresponding to the voltage of the programming pulse which first succeeded in raising the threshold voltage of one or more cells in the first set to or beyond the first intermediate threshold voltage.

14. The method according to claim 1, wherein the NVM cell is selected from the group consisting of Nitride Read Only Memory ("NROM"), multi-level cell ("MLC"), dual charge trapping region NROM, and dual charge trapping region MLC NROM.

15. A System for programming an array of non-volatile memory ("NVM") cells, said system comprising:

a controller adapted to cause a charge circuit to produce first phase programming pulses and to determine when one or more NVM cell of a first set of cells receiving the first phase programming pulses reaches or exceeds a first intermediate voltage, and to then cause said charge pump circuit to apply to a terminal the one or more cells in the first set second phase programming pulses adapted to induce relatively greater threshold voltage changes in cells having less stored charge than in cells having relatively more stored charge.

16. The system according to claim 15, wherein said controller is adapted to cause said charge pump circuit to initially apply to a terminal of one or more NVM cells of the first set of NVM cells first phase programming pulses having incrementally increasing voltage levels in concert with pulses of substantially fixed voltage applied to a gate of the one or more NVM cells, and once the threshold voltage of a one or more cells reaches or exceeds an intermediate threshold voltage level, said controller adapted to cause said charge pump circuit to apply to a terminal of one or more cells second phase programming pulses of substantially fixed voltage in concert with gate pulses of incrementally increasing voltage.

17. The system according to claim 16, wherein said controller is adapted to cause said charge pump circuit to initially apply to a terminal of one or more NVM cells of the first set of NVM cells first phase programming pulses of incrementally increasing voltage in concert with pulses of substantially fixed voltage applied to a gate of the one or more NVM cells, and once the threshold voltage of one or more cells reaches or exceeds an intermediate threshold voltage level said controller adapted to cause said charge pump circuit to apply to a terminal of one or more cells second phase programming pulses of incrementally increasing voltage in concert with gate pulses of substantially fixed and reduced voltage.

18. A multi-phase method of programming an array of non-volatile memory ("NVM") cells, said method comprising:

Applying to a first set of NVM cells first phase programming pulses; and

upon one or more NVM cells of the first set of cells reaching or exceeding a first intermediate threshold voltage level, applying to a terminal of one or more cells in the first set of cells second phase programming pulses adapted to induce deterministically lower programming rate for all cells in first set.

19. A System for programming an array of non-volatile memory ("NVM") cells, said system comprising:

a controller adapted to cause a charge circuit to produce first phase programming pulses and to determine when one or more NVM cell of a first set of cells receiving the first phase programming pulses reaches or exceeds a first intermediate voltage, and to then cause said charge circuit to apply to a terminal of the one or more cells in the first set second phase programming pulses adapted to induce a deterministically reduced programming rate.